AMENDMENTS TO THE CLAIMS

1. (Original) A method for analyzing an electromagnetic field of a circuit board based on shapes of conductor patterns and signal analysis conditions including steps of:

setting up initial shapes of conductor patterns in each layer of a multilayer circuit board;

setting up initial ports for input or output of an external signal in each conductor pattern;

dividing two-dimensionally the multilayer circuit board into a plurality of areas;

setting up additive ports on edges of the conductor pattern which has been created by area-division;

setting up individual analysis conditions for the initial ports and the additive ports, respectively;

performing an electromagnetic analysis of the multilayer circuit board by the divided area, based on the analysis conditions; and

integrating results of the electromagnetic analysis over each of the divided areas, thereby obtaining results of the electromagnetic analysis over the whole circuit board.

2. (Original) The method for analyzing an electromagnetic field of a circuit board according to Claim 1, wherein in the step of dividing the multilayer circuit board into a plurality of areas, the multilayer circuit board is divided two-dimensionally into a plurality of areas using dividing lines including a plurality of straight lines parallel to each other.

3. (Original) The method for analyzing an electromagnetic field of a circuit board according to Claim 1, wherein in the step of dividing the multilayer circuit board into a plurality of areas, the multilayer circuit board is divided two-dimensionally into a plurality of areas using dividing lines including a plurality of straight lines perpendicular to each other.

4. (Original) The method for analyzing an electromagnetic field of a circuit board according to Claim 1, wherein in the step of dividing the multilayer circuit board into a plurality of areas, the multilayer circuit board is divided two-dimensionally into a plurality of areas using dividing lines including a polygonal line or a curved line.

5. (Original) The method for analyzing an electromagnetic field of a circuit board according to Claim 1, wherein in the step of dividing the multilayer circuit board into a plurality of areas, shapes of the dividing lines are designated using a pointing device while representing a plan view of the multilayer circuit board on a display screen.

6. (Original) The method for analyzing an electromagnetic field of a circuit board according to Claim 1, including a step of calculating the number of the edges of the conductor pattern created by area-division.

7. (Original) The method for analyzing an electromagnetic field of a circuit board according to Claim 6, wherein in the step of setting up additive ports, the ports are added, the number of which corresponds to the calculated number of the edges.

8. (Original) The method for analyzing an electromagnetic field of a circuit board according to Claim 1, wherein in the step of setting up additive ports, the ports are added in the center of the edge.

9. (Original) The method for analyzing an electromagnetic field of a circuit board according to Claim 1, wherein, when a position of one port located on the edge of a conductor pattern residing in one layer coincides with a position of another port located on the edge of another conductor pattern residing in another layer, one of the ports is displaced to be represented on a display screen.

10. (Original) The method for analyzing an electromagnetic field of a circuit board according to Claim 1, including steps of:

changing the shape of the conductor pattern residing in a particular divided area, to perform again the electromagnetic analysis over the particular divided area; and

integrating a result of the electromagnetic analysis over the divided area with the result of the electromagnetic analysis over the another divided area, thereby obtaining results of the electromagnetic analysis over the whole circuit board.

11. (Original) An apparatus for analyzing an electromagnetic field of a circuit board based on shapes of conductor patterns and signal analysis conditions comprising:

means for setting up initial shapes of conductor patterns in each layer of a multilayer circuit board;

means for setting up initial ports for input or output of an external signal in each conductor pattern;

means for dividing two-dimensionally the multilayer circuit board into a plurality of areas;

means for setting up additive ports on edges of the conductor pattern which is created by area-division;

means for setting up individual analysis conditions for the initial ports and the additive ports, respectively;

means for performing an electromagnetic analysis of the multilayer circuit board by the divided area, based on the analysis conditions; and

means for integrating results of the electromagnetic analysis over each of the divided areas, thereby obtaining results of the electromagnetic analysis over the whole circuit board.

12. (Original) A circuit board with a rectangular shape comprising:

a plurality of layers having conductor patterns; and

a plurality of spiral inductance patterns provided in the conductor patterns;

wherein three out of the plurality of spiral inductance patterns are located on at least three of corner portions of the circuit board.

13. (Original) The circuit board according to Claim 12, wherein the spiral inductance pattern is located on each of the three corner portions of the circuit board so that the shortest distance L1 from the apex of the corner portion to the spiral inductance pattern and a diameter L2 of a circumcircle of the spiral inductance pattern satisfy a relation: $L1 \leq L2$.

14. (Canceled)

15. (Original) A method for designing a circuit board including a plurality of layers having conductor patterns in which a plurality of spiral inductance patterns are provided, including steps of:

dividing the circuit board into a plurality of divided areas using a dividing line; and

designing a circuit pattern over each of the divided areas using simulation,

wherein the dividing line is set up so as not to cut off two or more out of the plurality of spiral inductance patterns provided in the circuit board.

16. (Original) The method for designing a circuit board including a plurality of layers having conductor patterns in which a plurality of spiral inductance patterns are provided, according to Claim 15, wherein three out of the plurality of spiral inductance patterns are located on at least three of corner portions of the circuit board.

17. (New) A lamination device comprising:

the circuit board according to Claim 12; and

a semiconductor integrated circuit mounted on the circuit board.

18. (New) A lamination device comprising:

the circuit board according to Claim 13; and

a semiconductor integrated circuit mounted on the circuit board.